Claims

[c1] 1. A method for fabricating a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor channel region in a semiconductor substrate;

(b) forming a gate dielectric layer on top of the semiconductor channel region;

(c) forming a gate stack on top of the gate dielectric layer,

wherein the gate stack is electrically isolated from the semiconductor channel region by the gate dielectric layer,

wherein the gate stack comprises (i) a gate region on top of the gate dielectric layer, and (ii) a gate stack mask on top of the gate region,

wherein the gate stack mask comprises a gate mandrel and first and second gate spacers, and

wherein the gate mandrel is sandwiched between the first and second gate spacers;

(d) forming first and second source/drain regions in the substrate using the gate stack as an alignment mask;

(e) removing the first and second gate spacers;

(f) removing portions of the gate region beneath the removed first and second gate spacers; and

(g) filling a dielectric side plate material into spaces of the removed first and second gate spacers and the removed portions of the gate region beneath the removed first and second gate spacers so as to form first and second gate dielectric side plates.

[c2] 2. The method of claim 1, wherein the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer.

[c3] 3. The method of claim 1, wherein the semiconductor channel region is at a lower level than the gate region.

[c4] 4. The method of claim 1, wherein the step of forming the gate dielectric layer on top of the semiconductor channel region comprises the step of thermally oxidizing surfaces of the semiconductor substrate exposed to the atmosphere.

[c5] 5. The method of claim 1, wherein the dielectric side plate material comprises a low-K material.

[c6] 6. The method of claim 1, wherein the mandrel comprises silicon dioxide, and wherein the gate spacers comprise silicon nitride.

[c7] 7. The method of claim 1, wherein the step of forming the gate stack comprises the steps of:
forming a gate region layer on top of the gate dielectric layer, wherein the gate region layer comprises the gate region;
forming the gate stack mask on top of the gate region layer; and
using the gate stack mask as a mask to etch away portions of the gate region layer not covered by the gate stack mask so as to form the gate region.

[c8] 8. The method of claim 7, wherein the step of forming gate stack mask on top of the gate region layer comprises the steps of:
forming a gate mandrel layer on top of the gate region layer, wherein the gate mandrel layer comprises the gate mandrel;
patterning the gate mandrel layer so as to form the gate mandrel; and
depositing a gate spacer material on top of the entire semiconductor structure and then etching back so as to form the first and second gate spacers on side walls of the gate mandrel.

[c9] 9. The method of claim 1, wherein the step of forming the first and second source/drain regions comprises the step of doping by ion implantation the semiconductor substrate so as to form the first and second source/drain regions in the semiconductor substrate.

[c10] 10. The method of claim 9, wherein the step of forming the first and second source/drain regions further comprises the step of epitaxially growing a semiconductor material on top of exposed surfaces of the semiconductor substrate before the step of doping by ion implantation the semiconductor substrate.

[c11] 11. The method of claim 1, further comprising the step of removing the gate mandrel before the step of removing the first and second gate spacers.

[c12] 12. The method of claim 1, wherein the step of removing the first and second gate spacers comprises the steps of:
removing the gate mandrel;
depositing a dielectric material on top of the entire semiconductor structure;
planarizing a top surface of the semiconductor structure so as to expose top surfaces of the first and second gate spacers to the atmosphere; and
etching away the first and second gate spacers.

[c13] 13. The method of claim 1, wherein the step of removing the portions of the gate region beneath the removed first and second gate spacers comprises the step of etching vertically downward the empty space of the removed first and second gate spacers.

[c14] 14. A method for fabricating a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor channel region in a semiconductor substrate;

(b) forming a gate dielectric layer on top of the semiconductor channel region;

(c) forming a gate stack on top of the gate dielectric layer,

wherein the gate stack is electrically isolated from the semiconductor channel region by the gate dielectric layer,

wherein the gate stack comprises (i) a gate region on top of the gate dielectric layer, and (ii) and a gate stack mask on top of the gate region,

wherein the gate stack mask comprises a gate mandrel and first and second gate spacers, and

wherein the gate mandrel is sandwiched between the first and second gate spacers;

(d) removing the first and second gate spacers;

(e) removing portions of the gate region beneath the removed first and second gate spacers; and

(f) filling a dielectric side plate material into spaces of the removed first and second gate spacers and the removed portions of the gate region beneath the removed first and second gate spacers so as to form first and second gate dielectric side plates.

[c15] 15. The method of claim 14, wherein the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer.

[c16] 16. The method of claim 14, wherein the semiconductor channel region is at a lower level than the gate region.

[c17] 17. A semiconductor structure, comprising:

(a) a semiconductor channel region;

(b) a gate dielectric region being on top of the semiconductor channel

region;

(c) a gate region being on top of the gate dielectric region and being electrically isolated from the semiconductor channel region by the gate dielectric region; and

(d) first and second gate dielectric side plates being on top of the gate dielectric region and being on side walls of the gate region,

wherein the gate region is sandwiched between first and second gate dielectric side plates, and

wherein a top surface of the gate region is lower than top surfaces of the first and second gate dielectric side plates.

[c18] 18. The semiconductor structure of claim 17, wherein the first and second gate dielectric side plates comprise a low-K material.

[c19] 19. The semiconductor structure of claim 17, wherein the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer.

[c20] 20. The semiconductor structure of claim 17, wherein the entire gate region is at a higher level than the semiconductor channel region.